CLAIMS

1. A semiconductor integrated circuit, comprising:

a main circuit including a plurality of transistors of a MOS structure in which a source potential and a substrate potential are separated from each other, and operating while receiving a predetermined operating power supply voltage; and

a substrate potential control circuit for controlling the substrate potential of each MOS transistor of the main circuit, wherein:

a target saturation current value of the MOS transistor under the operating power supply voltage value of the main circuit is set in the substrate potential control circuit; and

the substrate potential control circuit controls the substrate potential of each MOS transistor of the main circuit so that an actual saturation current value of the MOS transistor under the operating power supply voltage value of the main circuit is equal to the target saturation current value.

2. The semiconductor integrated circuit of claim 1, wherein where a predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the target saturation current value of the MOS transistors of the main circuit is proportional to the operating power supply voltage value within the operating voltage range.

3. The semiconductor integrated circuit of claim 1, wherein where a predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range.

4. The semiconductor integrated circuit of claim 1, wherein:

the main circuit has a plurality of operating power supply voltage ranges;

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit; and

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range.

5. The semiconductor integrated circuit of claim 1, wherein the substrate potential control circuit controls the substrate potential of an nMOS transistor or that of a pMOS transistor among all the MOS transistors of the main circuit.

6. A semiconductor integrated circuit, comprising:

a main circuit including a plurality of transistors of a MOS structure in which a source potential and a substrate potential are separated from each other, and operating while receiving a predetermined operating power supply voltage; and

a substrate potential control circuit for controlling the substrate potential of each MOS transistor of the main circuit so that an actual saturation current value of the MOS transistor under the operating power supply voltage value of the main circuit is equal to a target saturation current value,

the substrate potential control circuit, including:

a constant current generation circuit;

a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value; and

a differential amplifier circuit for controlling a substrate potential of the current-voltage conversion circuit so that the converted voltage value from the current-

voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit,

wherein the substrate potential control circuit controls the substrate potential of each MOS transistor of the main circuit so that the substrate potential is equal to the substrate potential of the current-voltage conversion circuit controlled by the differential amplifier circuit.

7. The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is proportional to the operating power supply voltage value within the operating voltage range.

8. The semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range.

9. The semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges;

the constant current value of the constant current generation circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit; and

the linear function relationship between the constant current value of the constant current generation circuit and the operating power supply voltage value is different for each operating power supply voltage range.

10. The semiconductor integrated circuit of claim 6, wherein the constant

current generation circuit generates a plurality of constant current values, and selectively outputs one of the plurality of constant current values.

11. The semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the actual saturation current value of the MOS transistors of the main circuit.

12. The semiconductor integrated circuit of claim 11, wherein the constant current generation circuit includes an adjustment circuit for reducing variations in the generated constant current value.

13. A semiconductor integrated circuit, comprising:

a main circuit including a plurality of transistors of a MOS structure, and operating while receiving an operating power supply voltage; and

a power supply voltage control circuit for controlling the operating power supply voltage supplied to the main circuit, wherein:

a target saturation current value of the MOS transistors of the main circuit is set in the power supply voltage control circuit; and

the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current value of the MOS transistors of the main circuit is equal to the target saturation current value.

14. The semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is a target saturation current value of an nMOS transistor or that of a pMOS transistor from among the MOS transistors of the main circuit, or is an average value between the target saturation current values of the nMOS and pMOS transistors.

15. The semiconductor integrated circuit of claim 13 or 14, wherein the target saturation current value of the MOS transistors of the main circuit is in a linear function

relationship with the operating power supply voltage supplied to the main circuit.

16. The semiconductor integrated circuit of claim 13 or 14, wherein:

the main circuit includes a plurality of operating power supply voltage ranges;

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit;

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range.